Title: The Design of 100MSps 12Bit Pipeline SAR ADC

Abstract: This paper presents a 12-bit 100-MS/s two-stage SAR ADC in 65nm CMOS with a 1.2V supply. Compared to conventional single-stage designs, the proposed two-stage architecture reduces the capacitor array size by 50% and relaxes the comparator accuracy requirement by 4×. A 6+8 bit allocation with 2-bit inter-stage redundancy and an 8× residue amplifier is adopted, halving the theoretical gain to simplify the amplifier design. Both stages employ split-capacitor DACs and asynchronous SAR logic to shorten bit cycles. A bootstrapped switch and a double-tail comparator are used for high linearity and balanced speed-noise performance. Pre-layout simulation achieves an ENOB of 11.49 bits, an SNDR of 70.79 dB, an SFDR of 73.54 dBc, and a power consumption of 32.86 mW at 100 MS/s.