Title: A Weak FPGA PUF Utilizing Multiple-Parallel Delay-Line Time-to-Digital Converters with Histogram Method-based Linearity Self-Calibration

Abstract: This paper presents a weak FPGA PUF utilizing multiple-parallel delay-line Time-to-digital converter (MPDL-TDC) with histogram method-based linearity self-calibration. In measurement mode, the proposed PUF works as a high-resolution MPDL-TDC. In PUF mode, it works as a PUF that exploits delay of buffer of each stage of each TDC in MPDL-TDC as an entropy source. The proposed PUF generates a one-bit response output from the positive or negative of delay difference estimated from the histogram method-based calibration of a pair of buffers selected based on the challenge input. With a small amount of circuit, the proposed PUF can be applied to any type of MPDL-TDCs. Evaluation using 10 Artix-7 FPGAs resulted in an inter-chip Hamming distance of 47.07%, a reliability of 93.91%, and a uniformity of 50.70%. Extra resources for the proposed PUF over original MPSDL-TDCs is 2.44%.